REMARKS

I. Introduction

Claims 1-70 remain pending in this application. By this amendment, claims 1 and 69 are amended to correct minor typographical errors and claims 4 and 6 are amended to correct various formalities and improve clarity. Reconsideration, in view of the foregoing amendments and following remarks is respectfully requestsed.

II. Conferences with Examiners

Applicant appreciates the courtesies extended to Applicant's representative during the November 17 telephone conference with Examiner Teska and the November 19 telephone conference with Examiner Garcia-Otero. Applicant's response is based on the interpretation of the Office Action gleaned from these telephone conferences which is that, with respect to the art rejections, claims 1-18, 20-34 and 36-70 are rejected under 35 U.S.C. § 102(e) and claims 19 and 35 are rejected under 35 U.S.C. § 103(a).

III. Rejection under 35 U.S.C. § 112, 1st Paragraph

Claim 6 stands rejected under § 112, 1st paragraph. The Examiner asserts that the claim phrase "preventing the setting of interrupt flags from that point when the interrupt flags are cleared until the pipeline is stalled" is not enabled by the specification.

Applicant has amended claim 6 as follows: The method of Claim 2, further comprising, prior to stalling the pipeline, clearing any present interrupt enable flags, and preventing the setting of additional interrupt enable flags from the point when the interrupt enable flags are cleared until said pipeline is stalled. Therefore, by this amendment, it is clear that prior to

stalling the pipeline, interrupt enable flags are cleared. Then, the setting of additional interrupt enable signals is prevented until the pipeline is actually stalled. Exemplary support for this amendment can be gleaned, among other places, from p. 14, line 31 to p. 15 line 4 of the specification which states, ***"When the processor is in sleep mode, it is once again prepared to receive IRQs. Hence, IRQs are "blocked out" from that point when the interrupt flags are cleared until the sleep mode is entered. This is desirable in order to avoid the condition where an IRQ is being serviced after all interrupt flags have been cleared but before sleep mode is entered. IF such condition is allowed to occur, it would be possible for the processor to enter sleep mode with an interrupt flag set in memory."*** Thus, Applicant respectfully submitss that claim 6 as amended satisfies § 112, 1st paragraph. Accordingly, Applicant respectfully requests that the rejection of claim 6 be withdrawn.

IV. Rejection under 35 U.S.C. § 112, 2nd Paragraph

Claims 4, 6, 7, 11, 21 and 28 stand rejected under § 112, 2nd paragraph. Applicant respectfully traverses the rejection the basis of the following.

Regarding claim 4, the Examiner asserts that there is insufficient antecedent basis in parent claim 1 for the claim term "processor." Applicant respectfully submits that in embodiments of the present invention, the pipeline is stalled and memory is disabled thereby putting the processor in a reduced power consumption "sleep mode." Thus, it is clear from the specification that the steps of claim 1 effectively disable at least portions of the processor in order to reduce unnecessary power consumption. Though the processor is still operable to receive interrupts, the processor is halted from processing further pipelined instructions. However, for the sake of clarity and in order to expedite the prosecution of this application,

Applicant have amended claim 4 to recite that the pipeline is re-enabled after having been stalled. Accordingly, withdrawal of the rejection is respectfully requestsed.

Regarding claim 6, Applicant submits that the rejection has been rendered moot due to the amendment of claim 6 as discussed above in the context of the rejection of claim 6 under § 112, 1st paragraph. Accordingly withdrawal of the rejection is respectfully requested.

Regarding claim 7, the Examiner asserts that the claim phrase "providing a flag setting branch instruction" is indefinite because branching instructions appear distinct from flag setting instructions. The Examiner also asserts that the claim term "disposing" as it applies to the first instruction is indefinite. As to the first point, Applicant submits that a flag setting branch instruction is an instruction with a flag setting field that is set to be "on," thereby enabling interrupt flag setting. As illustrated in FIG. 1b, a SLEEP instruction may include a base instruction element 102, one or more operand fields 104 and one or more flag fields 106. As to the second point, Applicant respectfully submits that the term "disposing" is well understood and that this dependent claim merely further limits the location of the first instruction within a dealy slot in the flag setting branch instruction within the pipeline. Accordingly, the claim term is definite and no amendment is necessary to claim 7. Furthermore, this language is consistent with that used in claim 1. Accordingly, withdrawal of the rejection is respectfully requested.

In addition, in response to the Examiner's question at paragraph 21 of the Office Action, it is the flag setting jump instruction that restores the interrupt enable flags in the embodiment discussed at p. 15, lines 1-4. The sleep instruction is disposed in a delay slot of that instruction.

Regarding claim 11, the Examiner asserts the claim phrases "first and second enable signals" and "valid data" are indefinite. Applicant respectfully submits that first and second enable signals are described at p. 20, line 36 to p. 21, line 4 of the specification. Specifically,

this portion states that, ***"... the pipeline logic may be modified to prevent unnecessary switching activity – as discussed at pages 2-4 of the specification, switching activity increases power consumption – by (i) generating a low power version of the pipeline enable signal en1; and (ii) by generating the enable signal en2 which controls the data path to the ALU of the core. In the case of both the generation of en1 and en2, the modification comprises activating the two enable signals if the pipeline stage contains valid data."*** As discussed at p. 20, lines 33-35, data that is present in the pipeline that will not be used at a later state of the pipeline is subsequently invalid – valid data being data that will be used at a later state of the pipeline. Thus, the determination of validity is based on whether the data will be used at a later state. Therefore, Applicant submits that claim 11 satisfies the requirement of § 112, 2nd paragraph. Accordingly, withdrawal of the rejection is respectfully requested.

Regarding claim 21, the Examiner asserts that the claim phrase "detecting, using said logic circuit, that the predetermined condition exists with respect to certain of the data" is indefinite. Applicant respectfully traverses the rejection. In particular, Applicant submits that this claim refers to the embodiment discussed at pages 20-21 of the specification and is similarl to the claim features of claim 8, though no rejection was made of claim 8. The logic circuit detects whether the pipeline stage contains valid data as discussed above in the context of the rejection of claim 11. Further support for this is gleaned from claim 24, which depends upon claim 21, and which states ***"The method of Claim 21, wherein said act of detecting said predetermined condition of said data comprises using said logic circuit to detect when said data will not be used in a later stage of said pipeline."*** Thus, is clear that the predetermined condition of the data is that the data will not be used in a later state of the pipeline, thus rendering it invalid. Accordingly, withdrawal of the rejection is respectfully requested.

Regarding claim 28, Applicant respectfully requests withdrawal of the rejection on the same basis as that set forth in the traversal of the rejection of claim 11 as discussed above.

V. Rejections under 35 U.S.C. § 102(e)

Claims 1-18, 20-34 and 36-70 stand rejected under § 102(e) over U.S. Patent 5,996,083 to Gupta *et al.*(hereinafter "Gupta"). Applicant respectfully traverses the rejection. In particular, Applicant submits that Gupta fails to disclose or suggest a method of operating a pipelined digital processor having a memory, comprising defining a first instruction, said first instruction being adapted to stall the pipeline of said processor upon execution thereof, providing said first instruction within said pipeline, decoding said first instruction, executing said first instruction, stalling said pipeline in response to said first instruction, disabling said memory in response to said first instruction, and restarting said pipeline and enabling said memory upon the occurrence of a predetermined event, as recited in independent claim 1 and similarly recited in independent claims 36, 59, 68 and 70.

In contrast to the claimed invention, Gupta purports to disclose a heavily pipelined microprocessor having software-controllable power consumption that uses a power control register that includes a plurality of fields for individually controlling the power consumption of the individual functional units within the microprocessor. The configuration of Gupta purports to allow the microprocessor to shut down or adjust the execution rate of any one of the functional units when the software determines that the functional unit is not required by the currently executing software. In the system disclosed in Gupta, the pipeline is always functioning; only selected components, i.e., FPU, BPU, etc. are either shut down or supplied

with a scaled down clock signal, rather than stalling the entire pipeline. See col. 5, lines 47-56 for Gupta's definition of functional units. Gupta teaches away from pipeline stalling at col. 3, lines 1-13, which states that, ***"... the hardware has difficulty looking ahead to determine whether certain instructions are going to be issued. The detection circuitry can check the queued instructions in the instruction buffer; however, this provides an advance warning of only a limited number of instructions. This advance warning may be insufficient to have the functional unit fully operational before the instruction is executed. Thus, the pipeline must be stalled in order to allow the unit to wake up."***

Gupta does refer to pipeline stalling, but not as a means of saving power in a processor. At col. 9, lines 33-54, Gupta discloses that when power is reapplied to the functional unit , it may be several clock cycles before the functional unit can execute or perform its function. Thus, if an instruction is issued to it prematurely, the result will be erroneous. In order to prevent this from happening, the invention of Gupta includes logic within the functional unit to stall the microprocessor pipeline in the event that this condition occurs. Thus, pipeline stalling is only employed in Gupta as a means of delaying instructions that cannot be executed from reaching the particular functional unit before it is back "online." This points to the marked difference between the system disclosed in Gupta, and that of the claimed invention. Thus, Applicant respectfully submits that claims 1, 36, 59, 68 and 70 are patentable over Gupta on at least this basis.

In addition to independent claims 1, 36, 59, 68 and 70, the feature of stalling the pipeline is also common to the remaining independent claims, which can be functionally grouped into two categories: Category I, claims 21, 28 and 66; and Category II, claims 49, 55 and 69. Thus, theses claims are patentable over Gupta for at least the reasons set forth above

in the context of claims 1, 36, 59, 68 and 70. However, Applicant submits that the Category I and Category II claims also contain other significant features that are neither addressed by the Examiner nor taught in Gupta.

Regarding the category I claims, that is claims 21, 28 and 66, Applicant respectfully submits that Gupta fails to disclose or suggest a method of operating a pipelined digital processor having a logic circuit adapted for detection of a predetermined condition with respect to at least a portion of the data within said pipeline, comprising inserting a plurality of data into said pipeline, detecting, using said logic circuit, that the predetermined condition exists with respect to certain of said data, stalling said pipeline in response to said detected condition if no such pipeline stall is already invoked, checking for the presence of said condition at least once thereafter, and restarting the pipeline when said detected condition no longer exists, as recited in claim 21 and similarly recited in claims 28 and 66.

In contrast to the invention defined by claims 21, 28 and 66, Gupta teaches away from detecting whether a predetermined condition exists with respect to certain of the pipeline data, such as, for example, if the data is valid, that is, the data will be used in a later stage of the pipeline. Rather, instead of monitoring instructions, Gupta performs a comparison between an actual power latency register value stored in a functional unit and a corresponding power latency register field in the power latency register. See col. 9, lines 48-54. Therefore, Applicant respectfully submits that claims 21, 28 and 66 are patentable over Gupta on this basis, as well as the fact that Gupta does not stall the pipeline to reduce power consumption.

Regarding the Category II claims, that is claims 49, 55, 64 and 69, Applicant respectfully submits that Gupta fails to disclose or suggest a method of operating a digital processor core having a multi-stage pipeline, a program counter (PC), a plurality of core registers, a storage

device adapted to store a plurality of data therein, and a plurality of flags, including interrupt flags stored in said storage device, said processor core including an instruction set having at least one branch instruction and an associated delay slot, and at least one first instruction disposed in said delay slot and adapted to stall said pipeline upon execution, comprising, storing the settings associated with said interrupt flags in a first of said core registers, storing a destination address in said first core register, temporarily blocking new interrupt requestss, processing all said interrupt flags stored in said storage device, executing said branch instruction to branch to said first core register, updating said PC with said destination address, unblocking said interrupt requests, and executing said first instruction to cause said pipeline to stall with no interrupt flags set in said storage device, as recited in claim 49 and similarly recited in claims 55, 64 and 69.

In contrast to the claimed invention, Gupta does not teach branch instructions, nor does it disclose an associated delay slot, where an instruction disposed in the delay slot is adapted to stall the pipeline. The features highlighted above refer to a process for putting the processor in a sleep mode so that it is operable to receive interrupt requests, as discussed in part at pages 14-15 of the specification of this application. Interrupt requests are blocked out from the point when the interrupts flags are cleared until the sleep mode is actually entered. The reason for this is to avoid the condition where an IRQ is being serviced after all interrupt flags have been cleared but before sleep mode is entered. If this condition occurs, it would be possible for the processor to enter the sleep mode with an interrupt flag set in memory, even though the memory is required to be cleared before entering the sleep mode. Thus, to avoid this, the sleep instruction is disposed in a delay slot of a flag setting jump instruction that restores the interrupt enable flags. So interrupt enable flags are restored just

prior to entering the sleep mode. Because the system of Gupta does not stall the pipeline, Gupta is not relevant to the features disclosed in claims 49, 55 and 69. Applicant strenuously disagrees with the Examiner's assertion at paragraph 101 of the Office Action that states that all limitations of claims 41-70 are disclosed by Gupta. Moreover, Applicant submits that this wholesale rejection, which fails to address the specific features of these claims as discussed above, fails to establish a prima facie case of non-patentability with respect to these claims. Therefore, Applicant respectfully submits that claims 49, 55, 64 and 69 are patentable over Gupta for at least these reasons.

Applicant notes that though the Examiner's rejections under § 102(e) have been traversed in the context of the independent claims, dependent claims 2-18, 20 , 22-27, 29,34, 37-48, 50-54, 56-58, 60-63, 65 and 67 are submitted as patentable over Gupta for at least the same reasons as independent claims 1, 21, 28, 36, 49, 55, 59, 64, 66, 68, 69 and 70. Accordingly, based on the foregoing, Applicant respectfully requests that the rejection of claims 1-18, 20-34 and 36-70 under 35 U.S.C. § 102(e) be withdrawn.

VI. Rejection under 35 U.S.C. § 103(a)

Claims 19 and 35, stand rejected under § 103(a) over Gupta in view of U.S. Patent to Su (hereinafter Su). The Examiner relies on Su to teach features of dependent claims 19 and 35 relating to Gray Coding. The Examiner alleges that Su teaches limiting the number of bits in a binary sequence present within said data that change per clock cycle to a predetermined number. Without addressing the propriety of this allegation, Applicant respectfully submits that Su, as relied upon by the Examiner, fails to supply the many deficiencies of Gupta with respect to independent claims 1 and 28 as discussed above, nor, in

the case of claim 19, the features of intervening claim 18. Therefore, Applicant respectfully submits that claims 19 and 35 are patentable over the combination of applied references for at least the same reasons as claims 1 and 18. Accordingly, Applicant respectfully requests that the rejection of claims 19 and 35 under 35 U.S.C. § 103(a) be withdrawn.

VII. Conclusion

Applicant submits that for at least the reasons set forth herein above, all claims of the present application are in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

Dated: November 22, 2004 By: _____

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